PATENT
Docket No.: 016491-002710US
Client Ref. No.: PMC-981041

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No.: 6523
Heng Liao	Examiner: Hussein A. El Chanti
Application No.: 09/538,132	Art Unit: 2157
Filed: March 29, 2000	DECLARATION OF HENG LIAO UNDER 37 C.F.R. SECTION 1.132
For: METHOD AND APPARATUS FOR PROGRAMMABLE LEXICAL PACKET CLASSIFIER	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

I, Heng Liao, hereby declare and state:

1. I earned a Bachelor of Science degree in Computer Science & Technology from the Tsinghua University in Beijing, China, in 1992; a Master of Science degree in Computer Science & Technology from the Tsinghua University, in 1996; and a Ph.D. in Computer Science from the Tsinghua University, in 1996.
2. I held a post-doctoral post at Princeton University from 1996 to 1997, and conducted research in compiler techniques and parallel processor architectures.
3. I am currently employed by PMC-Sierra, Inc., a Canadian company and the assignee of the present Patent Application, and have been in its employ since 1997. My current job title is Principal Engineer. I have over 15 years of experience in the field of Computer Science, Computer Engineering and VLSI design.
4. I currently serve as an Adjunct Professor at the Tsinghua University, where I teach two times a year, for two weeks at a time.
5. Attached as Exhibit 1 is my curriculum vitae.

6. I am the sole inventor of U.S. Application No. 09/538,132, filed March 29, 2000, entitled "METHOD AND APPARATUS FOR PROGRAMMABLE LEXICAL PACKET CLASSIFIER" (hereinafter "the present Patent Application").

7. I have reviewed the final Office action mailed on February 23, 2006 in the present Patent Application and am very familiar with the cited art. It is my understanding that the claims 1-4, 11-12, 18-22, 47, and 50 stand rejected for being anticipated by Hekhuis (U.S. Pat. No. 5,414,650, hereinafter "Hekhuis"). It is my further understanding that the claims 5-10, 13-17, 23-45, 48-49, and 51-54 were rejected as being obvious in view of Hekhuis and Narad et al. (U.S. Pat. No. 6,701,338, hereinafter "Narad"). However, as to independent claims 23, 31, 40, and 51, it is my understanding that the examiner relies on Narad for the DFA aspect of the claims and that Hekhuis is relied on for all of the other aspects of the claims.

8. Based on my 15 years of experience and training in the field of compiler techniques, it is my conclusion after a review of Hekhuis that he does not disclose providing a language definition and processing network data by scanning the network data using lexical token scanning in accordance with a formal language processing technique to classify data packets (see independent claims 1, 23, 31, and 40). Hekhuis does not disclose providing a language definition and processing network data by matching it against regular expressions to classify data packets (see independent claims 11, 47, and 51).

9. Hekhuis discloses a "loseless compression scheme" similar to Lempel-Ziv (LZ compression) and is often referred to as "dictionary based compression" or "a substitutional compression scheme." See column 1 line 45-70. The general idea: parse an input stream, and build a dictionary of "vocabulary," which are "substrings" that show up frequently in the original input and map these vocabulary to "tokens." The dictionary is updated as the processor parses through the input stream, collecting information about which "substring" is frequently used. Thus, by replacing the most frequently used vocabulary with shortest encoding, the original text string is represented by the dictionary + the string token. Since the dictionary is constructed on the fly, it does not consume any storage space. The tokens are encoded with an efficient code, and the size of the text is now compressed.

10. Responding to the examiner's assertions made in the final Office action on page 17, Hekhuis' string matching with the set { "and", "br", "d", "f", "ing", "th" } does not constitute a grammar of a language definition. Hekhuis does not teach "a language definition" that includes a "grammar." In fact, it appears from my review of Hekhuis that he makes no mention at all of a grammar. Furthermore, Hekhuis' "dictionary" does not constitute a formal language. As discussed above, Hekhuis' dictionary is a table of substrings of the original text to be compressed and corresponding replacement text called the "token."

11. Responding to the examiner's reliance of Hekhuis in column 8, line 55 to column 9, line 37 and column 10, line 40 to column 11, line 42 for his rejection of independent claims 1, 6, 11, 18, and 27, the parsing process described by Hekhuis does not utilize lexical token scanning (regular expression). In fact, it appears from my review of Hekhuis, that he makes no mention at all of regular expressions or lexical scanning. Instead, Hekhuis describes using intrinsic rules (cardinal vs. collateral classes), and transition rules (as outlined in col. 8 lines 55-65 for packet boundary identification). Neither the intrinsic rules nor the transition rules have any lexical or grammatical significance.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under § 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date Aug 18. 2006

Heng Liao, Ph.D.

EXHIBIT 1

CURRICULUM VITAE

Heng Liao
Principle Engineer, Product Research
PMC-Sierra, Inc

EDUCATION

1987-1996 Tsinghua University Beijing, China

- Enter the university at the age of 14.
- B.S.E. in Department of Computer Science & Engineering. (1992)
- Ph.D. in Department of Computer Science & Engineering. Thesis title: A study on high speed network switch and interface for cluster parallel computing. (1996)

1996-1997 Princeton University Princeton, New Jersey.

- research scientist (Research Associate) in computer engineering group in Department of Electrical Engineering.

WORK EXPERIENCES

- Five years of computer software, hardware and system design experience as the leader of an independent research & development team as a college student (1989-1994).
- Two years of computer products development in Creative Research Center (Creative Technology Ltd. Based in Singapore) as Product Manager and Chief Engineer(1994-1996).
- Research Scientist at Princeton University.
- Seven years of VLSI design, leader and architect experience (Senior Design Engineer, , Leader, Technical Advisor and Principle Engineer) at PMC-Sierra, Inc. (1997-Now)

PROJECTS

1987-1996 Tsinghua University Beijing, China

As an Undergraduate and Graduate Student

- A speaker-independent connected digit speech recognition system for voice telephone dialling. The system is based on PC and TMS320c25 hardware. Hidden Markov Model is used to set up a speech model. A high level search algorithm is developed to find the maximum likelihood path. (1992)

- A 1GBps High speed network switch and interface based on Altera FPGA for cluster parallel processing. The system is design to resolve the communication latency and overhead in networked parallel processing system. The project implements a network switch with 8 1Gbps bi-directional ports with switching latency less than 200ns. Special network interface is design to reduce the software protocol overhead to transfer data between main memory and network interface. (1996)

1989-1996 As an Independent Developer

- A TV wall controller which can display real-time video image on a large screen consists of 4x4 TV sets. Phillips digital video decoder chipset was used to digitize the standard video signal. Hardwired logic was design to enlarge and distribute the real-time digital video data to different frame buffers and
- generate synchronization signals. Scaleable structure was used to enable the system to support larger array. (1992)
- A DSP board based on TI TMS320c25. The board was design to support digital speech signal processing and recognition. Laser printer and imagesetter interfaces were added to the board later to support fast rendering or Chinese fonts and was used as a low end imagesetter controller. (1994)
- An Intel 80960CA based Postscript laser printer. The hardware system includes a 33Mhz 80960CA processor, 16M bytes of memory, Canon LBP family laser printer interface, an IDE hard disk interface, and a network interface. BIOS firmware was developed to support the basic operations of the interfaces and hard disk. Postscript and HP-PCL interpreters was developed and embedded as part of the printer firmware. It took me more than one year to finish this project. (1994-1995)
- A MPEG decoder board based on C-Cube CL450. An ADSP 2015 processor was used as an audio decoder.
- A RIP (Raster Image Processor) which controls a high resolution imagesetter to produce color separation films for high quality color press printing. The RIP was based on the technologies of the Postscript printer controller. Some improvement was made to support higher resolution(3048) and larger page size(ISO A2). Memory compression technology was developed to reduce memory size requirement and support real-time transfer of image data between RIP and the imagesetter. The RIP was used to control the ECRM VR-36 imagesetter. Chinese patent was granted. (1996)
- A palm-top wheat moisture-meter. The system is based on the non-linear relationship between the capacitor of certain amount of wheat and the moisture. An Intel 8031 microprocessor and a capacitor measurement circuit were used. Power saving techniques were developed to save battery life.

Chief Engineer/Project Manager, Creative R&D Center, Beijing

- Helped Creative Technologies (Singapore) to set up the Creative Research Center in China. (1994)
- Creative Hansware 1.0 office software package including a MS-Word like word processor, an optical character reader, an translation software and a MS-Windows patch to support Chinese characters. I managed a team of 5 developer and 2 tester in

this project. About 200k lines of C++ code was produced, I finished more than 60k lines alone. (1994-1995)
- Creative Hansware 95 office software package which is an updated version to support Windows 95. (1995-1996)

1996-1997 Princeton University Princeton, NJ

- Postdoc (Research Associate) in EE department
- Design the arithmetic instruction set of a VLIW video signal processor.
- Design the DMA engine for the video signal processor.
- C-language optimizing compiler for the VSP
- Studied the instruction level parallelism in video applications.
- Design the layout of on-chip memory of VSP.

1997-NOW PMC-Sierra, Inc. , Burnaby, BC

- Design ARL system block for EAGLE/FELIX gigabit Ethernet Switch port controller
- Top level integration/verification of EAGLE/FELIX gigabit Ethernet Switch port controller
- Architect, research/feasibility work in IP layer network processor/classifier device.
- Architect, research/feasibility work in Diffserv IP traffic manager device
- Architect, TAP-3200 project, a network processor datapath element
- Standards Representative, IEEE 802.17 Resilient Packet Ring Protocol
- Standards Representative, Internet Engineering Task Force, IP Security Working Group
- Standards Representative, Metro Ethernet Forum
- Architect, research/feasibility work in 802.17 RPR MAC device
- Architect, research/feasibility and product definition in ARROW 2xFE, 2 port Ethernet over SONET mapper device
- Architect, research/feasibility and product definition in ARROW 24xFE, 24 port Ethernet over SONET mapper device
- Architect, research/feasibility in Layer 2 Product Area and LINX-10G product
- Standards Representative, ANSI T10 (Serial Attached SCSI) working group
- Standards Representative, SATA working group
- Architect, research/feasibility and product definition in SAS Expander device (SXP12 and SXP36/24 devices)
- Research work in TCP Offload Engine
- Architect, Serial Attached SCSI RAID controller (SRC8x6G)
- Chief Architect for Enterprise Storage Division

2002-NOW Tsinghua University

- Adjunct Professor, Department of Computer Science & Technology, Tsinghua University, Beijing, China.

PATENTS (GRANTED AND PENDING IN US AND CANADA)

- CA2311078, Multithreaded Address Resolution System
- US09471263 Multithreaded Address Resolution System
- US09557736 Method and Apparatus for Grammatical Packet Parser - Non-Provisional
- CA2307529 Method and Apparatus for Grammatical Packet Parser - Non-Provisional
- US09538132 Method and Apparatus for Programmable Lexical Packet Classifier - Non-Provisional
- CA2306364 Method and Apparatus for Programmable Lexical Packet Classifier - Non-Provisional
- US09908917 Multi-Field Classification Using Enhanced Masked Matching
- US09953215 Two-Step Enhanced Masked Matching Algorithm for Multi-Field Classification
- CA2356572 Transmit Virtual Concatenation Processor
- US09943886 Transmit Virtual Concatenation Processor
- US60316375 Sonet Virtual Concatenation Receive Processor with Differential Delay Alignment
- US60265105 Feedback Priority Modulation Rate Controller - Non-Provisional
- A Method and Apparatus for Queuing Variable Size Packets in Block-Transfer Memories(Filed 2002, US patent number to be issued by USPTO)
- Marriage Network for Data Stream Permutation of Large Dimension (Filed 2002, US patent number to be issued by USPTO)
- Sonet Virtual Concatenation Receive Processor with Differential Delay Alignment - Non- Provisional (Filed 2002, US patent number to be issued by USPTO)
- Generic Packet Parser Patent Disclosure (Filed 2002, US patent number to be issued by USPTO)
- VLAN grooming and aggregation (Filed 2003, US patent number to be issued by USPTO)
- Multiport Register File (Filed 2003, US patent number to be issued by USPTO)
- Cache Queuing (Filed 2003, US patent number to be issued by USPTO)

PUBLICATIONS

- "Hardware Support for Process Synchronization", Microcomputer and Minicomputer System Journal, Vol. 16, No. 9, Sept. 1995.
- "Virtual Register and Parallel Instruction Processing Unit", Microcomputer and Minicomputer System Journal, Vol. 16, No. 6, June 1995.
- "A Virtual Shared Memory Multiprocessor System with Distributed Memory and Private Consistent Caches", IEEE International Conference of Young Computer Scientists, 1995
- "Hardware Support for Process Synchronization Algorithms on I860XP Based Multiprocessor System", IEEE International Conference of Young Computer Scientists, 1995

- "Trace Merging Scheduling", IEEE International Conference of Young Computer Scientists, 1995
- "DYNAMEM - A Micro-architecture for Improving Memory Disambiguation at Run-time", Journal of Computer Science and Technology, 1996
- "Virtual Register Architecture", Journal of Computer, 1996
- "A Survey of VSP", Princeton University Technical Report, 1996
- "Five Hand Scheduled VSP programs", Princeton University Technical Report, 1996
- "VSP DMA Engine Design", Princeton University Technical Report, 1997
- "Available Parallelism in Video Applications", IEEE MICRO'97, 1997